ABSTRACT OF THE DISCLOSURE

An improved Finite Impulse Response (FIR) filter is presented which provides linear scalability and implementation without the need for delay lines. A multiprocessor architecture includes a plurality of ALUs (Arithmetic and Logic Unit), Multipliers units, Data cache, and Load/Store units sharing a common Instruction cache. A multi-port memory is also included. An assigning functionality assigns to each available processing unit the computation of specified unique partial product terms and the accumulation of each computed partial product on specified output sample values.